FEDEVEL

CERTIFICATION

This is to certify that

JOSE LUIS FERNANDEZ BAENA

has successfully completed the course

Essential PCB design/layout techniques for good EMC

Date **9 MAY 2025**

Course tutor *Keith Armstrong*

Keith Armstrong

Course duration: 5h 25min **Course content:** Saving time and money, Scope and application of these design techniques, EM Zoning (i.e. segregation), Interface analysis, filtering, and suppression), Planes for 0V(GND) and other power rails (PWR), RF-bonding PCB Reference Planes at EMZ boundaries, Power supply decoupling, Switching power converters (AC/DC, DC/DC, DC/AC, etc.), Matched transmission line techniques, Layer stacking and trace routing, Devices with BGA packages and/or multiple DC rails, Some useful references, sources, and webinars

www.fedevel.com

Certificate number: 1a77486c7943350b693a8d660