



CERTIFICATION

This is to certify that

Javier García Rodríguez

has successfully completed the course

VHDL and FPGA Development

Date **13 MAR 2026**

Course tutor

Jordan Christman



Jordan Christman

Course duration: 17h 40min **Software used:** Vivado, Quartus **Course content:** Creating a new project, Understanding VHDL, Creating and simulating VHDL design, Setting up and working with FPGA pins, AD processing, Building complex designs, Implementing: PWM, UART, SPI and I2C in FPGA.