FEDEVEL

CERTIFICATION

This is to certify that

Dimitrios Malamas

has successfully completed the course

VHDL and FPGA Development

Date **13 JAN 2025**

Course tutor *Jordan Christman*

Jordan Christman

Course duration: 17h 40min **Software used:** Vivado, Quartus **Course content:** Creating a new project, Understanding VHDL, Creating and simulating VHDL design, Setting up and working with FPGA pins, AD processing, Building complex designs, Implementing: PWM, UART, SPI and I2C in FPGA.

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Certificate number: 196e960d233e5a9e6646275d2